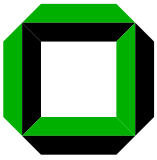

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System Architecture 2008/09
Assignment 16

Hint: A discussion of this assignment will take place on Friday, March 20, 2009 in HSaF at 9 am.

Q16.1: Kernel Entry (6 marks)

Enumerate the three different types of events that trigger a mode-switch from user mode to kernel mode. Give typical examples for each of these events. Enumerate all types of activities that run in kernel mode.

Q16.2: Mutual Exclusion (4 marks)

Enumerate all necessary and two desirable requirements for a valid solution for a mutual exclusion problem. Explain the terms *Critical Region* and *Critical Section*. What is a *Nested Critical Section*? Discuss problems with nested critical sections.

Q16.3: POSIX System Calls (10 marks)

Enumerate the ten most frequent system calls that allow a portable managing of the different types of activities. Make proper assumptions and reason your choice. Describe in short what the mentioned system calls are doing. Some system calls are functions whose return values characterize the degree of successfulness. What return value is usually given provided the system call was successful? Why is parameter control of system calls so important?

Q16.4: HW & SW Assumptions and Additional Requirements(10 marks)

To reduce the complexity of the course topics we have made some simplifying assumptions about HW & SW. What system components are depending on those assumptions? On the other hand, we also have introduced additional requirements into the multi-dimension design space. Discuss this topic as a KIT student.

Q16.5: Deadlocks and DIMMUNIX (5 marks)

Dimmunix assumed that all *critical sections* are protected via locks of type mutex. Characterize what a mutex is and evaluate its principal deadlock probability compared to other coordination objects. Assume you have a multi-threaded application with $n \gg 1$ KLTs, each of which might have multiple and different critical sections. Is it possible that a deadlock can occur, if none of these KLTs uses nested critical sections? Under what conditions can one of these KLTs starve? Suppose DIMMUNIX has detected a deadlock caused by KLT1 and KLT2 at the mutex1 and the mutex2. How does DIMMUNIX prevent that this specific deadlock will occur again? Does DIMMUNIX guarantee that neither KLT1 nor KLT2 will deadlock again? Does DIMMUNIX guarantee that neither at mutex1 nor at mutex2 another deadlock will occur?

Q16.6: Corbato Paper (3 marks)

What have been the design errors in CTSS that allowed normal users to read the password file instead of the message of the day? What was the major lesson learnt from MULTICS? Enumerate some conclusions how to design future systems that might contain fewer failures?

Q16.7: Multiple Choice (6 marks)

1. Putting blocks of a file, which are likely to be accessed in sequence, close to each other results in

(a) smaller files (b) reduced disk arm motion (c) less disk space wasted
(d) all of these (e) none of these

2. Files whose entities can be read in any order are called
   (a) sequential access (b) random access (c) binary
   (d) executable (e) all of these (f) none of these

3. How are files structured?
   (a) sequence of records (b) tree of records (c) all of these

4. What concept allows multiple executions to take place in the same application environment, more or less independently?
   (a) interrupts (b) PCBs (c) threads
   (d) kernel (e) none of these (f) all of these

5. A place to buffer a certain number of messages is called
   (a) mailbox (b) semaphore (c) barrier synchronization
   (d) rendezvous (e) none of these (f) all of these

6. In Unix all I/O devices are made to look like
   (a) arrays (b) files (c) keyboard streams
   (d) registers (e) none of these (f) all of these

Q16.8: Single Choice, only one answer is correct) (4 marks)

1. Which of the following attributes is not part of a Linux Ext2 file?
   (a) File length
   (b) Number of symbolic links
   (c) Access rights
   (d) Owner

2. Which attributes does an Ext2 directoy entry contain?
   (a) Block number of inode-disk block and file name
   (b) Inode number and file name
   (c) File name, block number of first file block, file size, owner and access rights
   (d) Only inode number

3. When using a priority based scheduling you might run into problems. Which of the following problems can arise?
   (a) The number of priorities is not enough, when there are only few processes.
   (b) Processes might starve.
   (c) The phenomenon priority inversion might lead to starvation of low-priority processes.
   (d) The scheduling policy works inefficiently, when there are many ready processes.

4. The typical standard page frame size is
   (a) 8 — 32 bytes
   (b) 512 — 8192 bytes
   (c) 64 KB — 4 MB

Q16.9: File System Cache (5 marks)

1. What is the basic idea of a file system cache in main memory?
2. Some systems offer read ahead. Discuss pros and cons.
3. What other methods are used to improve disk throughput?

Q16.10: Scalability (2 marks)

One of the design goals for a new OS could be scalability. Discuss some concepts that support scalability, and some mechanism that reduce scalability.

Q16.11: Extensible Hashing (3 marks)

1. Describe the major meta data of an extensible hashing-file. Assume you want to support efficiency when accessing an extensible hashing file. What could you do?
2. Can you get all records of an extensible hashing-file efficiently? If so, tell how. If not, show, why not.

Q16.12: Page Table & Translation Look aside Buffer Entries (6 Marks)

Explain the purposes of the following fields of a page table entry (PTE) respectively TLB entry.

(a) Physical address	(b) Presence bit	(c) Reference bit
(d) Dirty bit	(e) Pin bit	(f) Cache disable-bit

Which of these fields are accessed by what kind of HW unit or SW components with either HW or SW managed TLBs?

Q16.13: Inverted Page Table (5 marks)

1. Enumerate the necessary entries of an inverted page table for a multi-programming system.
2. Describe the address transformation with an inverted page table.
3. Suppose, one page is currently not mapped. Where do you place the corresponding peripheral address of that page?

Q16.14: Just for Fun

You have to design an online game that simulates different naval battles consisting of WW2 and modern ships. Each ship has one commanding officer. During the game each combat side can add or withdraw ships and officers. What activity model would you install provided all thread models are supported by all involved systems?